Table of Contents

欢迎辞 Welcome Message 02

会议日程 Conference Schedule 03

组委会 Conference Committee 05

会议地点 Conference Venue 06

参会指南 Guideline & Tips 07

会议讲座 Tutorial 08

线下分会 Afternoon Session 1 09

线下分会 Afternoon Session 2 12

线上分会 Online Session 15

Welcome Message

Dear Delegates,

It is our great pleasure to welcome you to Ningbo, China, for the 2026 6th International Conference on Circuits, Systems and Devices (ICCSD 2026), held from November 13 to 15, 2026. ICCSD provides a forum for researchers and scholars from universities and research institutions to meet, exchange ideas, and share recent progress in the broad fields of circuits, systems, and devices.

Rapid advances in semiconductor technologies, integrated circuits, sensing, computing, and system integration are continuously reshaping modern electronic systems and creating new research opportunities across multiple disciplines. Against this background, ICCSD 2026 brings together research covering microelectronic devices, power devices and power management, sensors and displays, electromagnetics and microwave devices, 3D integration and microsystems, as well as digital VLSI and memory systems. The conference also welcomes discussions on emerging areas such as wide-bandgap semiconductor devices, terahertz technologies, heterogeneous integration, in-memory computing, AI hardware, hardware security, and emerging post-CMOS technologies.

Through these diverse research areas, ICCSD 2026 seeks to encourage the exchange of new ideas, research methods, technical developments, and practical experience among participants from different universities and research institutions. We hope the conference will provide opportunities for researchers working at different levels of devices, circuits, and systems to better understand related developments, identify common challenges, and explore possibilities for future research and collaboration.

The conference program includes tutorial, invited talks, and oral presentations covering a variety of topics related to circuits, systems, and devices. We encourage all participants to engage actively in the presentations and discussions, exchange perspectives with fellow researchers, and make full use of the conference as a platform for academic communication.

We would like to express our sincere appreciation to the organizing committee members, technical program committee members, reviewers, speakers, authors, and all those who have contributed their time and effort to ICCSD 2026. We also thank every delegate for your participation and support. Your research contributions and active involvement form an essential part of the academic exchange that this conference seeks to promote.

On behalf of the organizing committee, we warmly welcome you to ICCSD 2026. We hope that your time in Ningbo will bring productive discussions, new ideas, and valuable connections, and we wish you an enjoyable and rewarding conference.

Sincerely,
Organizing Committee of ICCSD 2026

Conference Schedule

DAY 1 November 13 | Friday

11:00-12:00	Test for Online Session	线上报告测试	ZOOM ID: 848 3029 5608

DAY 2 November 14 | Saturday

3 楼，君悦厅（Jun Yue Hall, 3F）		
Host: Zhufei Chu, Ningbo University, China		
09:00-10:20 (上半场)	**Tutorial**: Prof. Christos P. Sotiriou, University of Thessaly and Silicon Highway Technologies GP, Greece *Speech Title: The refEDA Tool Suite*	
10:20-10:40	Coffee Break	
10:40-12:00 (下半场)	**Tutorial**: Prof. Christos P. Sotiriou, University of Thessaly and Silicon Highway Technologies GP, Greece *Speech Title: The refEDA Tool Suite*	
12:00-13:30	Lunch Time	**6 楼，608（Room 608, 6F）**
Host: Weikang Qian, Shanghai Jiao Tong University, China		
13:30-14:00	**Invited Speech 1: Kang Zhao, Beijing University of Posts and Telecommunications, China** 赵康，北京邮电大学 *报告题目：《FPGA 的敏捷设计与智能设计》*	
14:00-14:20	**Invited Speech 2: Yuanqing Cheng, Beihang University, China** 成元庆，北京航空航天大学 *报告题目：基于 2.5D/3D 集成电路的仿真与验证*	
14:20-14:40	**Invited Speech 3: Yujie Wang, Institute of Computing Technology, Chinese Academy of Sciences, China** 王郁杰，中国科学院计算技术研究所 *报告题目：芯粒处理器架构-封装协同设计*	
14:40-14:55	**Oral Presentation: D2489 | Ninghuang Li, Peking University, China** *Title: A 48V to 2 ~ 5 V 95.1%-Peak-Efficiency Dual-Path Fibonacci-based Hybrid Converter with Inductor Current Reduction*	
14:55-15:10	**Oral Presentation: D5767 | Zhenhao Guo, Ningbo University, China** *Title: A Neural Encryption IP Core with Joint Adversarial Training Against Four Types of Attackers*	
15:10-15:40	Break Time	
Host: Yuanqing Cheng, Beihang University, China		
15:40-16:00	**Invited Speech 5: Xiaole Cui, Peking University ShenZhen Graduate School, China** 崔小乐，北京大学深圳研究生院 *报告题目：Chiplet 互连测试与修复技术进展*	
16:00-16:20	**Invited Speech 6: Weikang Qian, Shanghai Jiao Tong University, China** 钱炜慷，上海交通大学 *报告题目：机器学习辅助的逻辑综合*	

16:20-16:40	**Invited Speech 7: Xiaohang Wang, Zhejiang University, China** 王小航，浙江大学 *报告题目：集成芯片仿真方法与设计空间探索*	
16:40-17:00	**Invited Speech 8: Xueyin Zhang, Shanghai Hongxin Micro Nano Technology Co., Ltd., China** 张雪垠，上海鸿芯微纳技术有限公司 *报告题目：鸿芯微纳 Komponist® 3DIC 设计平台*	
17:00-17:15	**Oral Presentation: D9170 | Zhenghe Wang, Wenzhou University, China** *Title: A 75 F² Leakage-Current Based Physically Unclonable Function With Unstable-Bit Screening Function*	
17:15-17:30	**Oral Presentation: D7164 | Baomin Tang, Ningbo University, China** *Title: A Four-Coefficient-Parallel BRAM-Free NTT Architecture With Dual-Bank Commutation and Interstage Overlap for ML-DSA*	
18:20-20:00	Dinner Time	**3 楼，君悦厅（Jun Yue Hall, 3F）**

DAY 3 **November 15 | Sunday**

ROOM ID: 848 3029 5608 **ROOM Link: https://us02web.zoom.us/j/84830295608**

16:00-16:15	**Oral Presentation: D1846 | Jingwu Gong, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, China** *Title: A Compact Incremental Delta-Sigma ADC for Column-Parallel Terahertz Readout*
16:15-16:30	**Oral Presentation: D8113 | Xiaoyu Zhong, The 58th Research Institute of CETC, China** *Title: Design of a High-Speed and Low-Power Readout Circuit for UTBB-Based Image Sensors*
16:30-16:45	**Oral Presentation: D4653 | Bin Wang, Shenyang University of Technology, China** *Title: A High-Voltage High-Slew-Rate Rail-to-Rail Operational Amplifier with Constant Transconductance*
16:45-17:00	**Oral Presentation: D4560 | Haojie Huang, University of Bristol, United Kingdom** *Title: PCB Design and Verification of an MP4560-Based DC-DC Step-Down Module*

Conference Committee

Conference Chairs

Yuhua Cheng, Peking University, China

Jian Wang, Ningbo University, China

Conference Co-chair

Zhufei Chu, Ningbo University, China

Program Chairs

Zhao Zhang, Institute of Semiconductors, Chinese Academy of Sciences, China

Jinping Zhang, University of Electronic Science and Technology of China, China

Fanyi Meng, Tianjin University, China

Program Co-chair

Fakhrul Zaman Rokhani, Universiti Putra Malaysia, Malaysia

Publicity Chairs

Zenglong Zhao, Tianjin University, China

Ming Zhang, Hubei University, China

Yushi Zhou, Lakehead University, Canada

Technical Committee

Ljiljana Trajkovic, Simon Fraser University, Canada

Nikolaos Anagnostopoulos, University of Passau, Germany

Dimitrios Soudris, National Technical University of Athens, Greece

Janelli M. Mendez, Lorma Colleges – Carlatan Campus, Philippines

Jian Zhu, Nanjing University, China

Bo Jiang, Omni Vision Technologies, USA

Chunyu Peng, Anhui University, China

Yu Xiao, Sun Yat-Sen University, China

Tiedong Cheng, Jiangxi University of Science and Technology, China

Deming Zhang, Hefei Innovation Research Institute, Beihang University, China

Paul Zhou, Analog Devices, USA

Kostas Siozios, Aristotle University of Thessaloniki, Greece

Mei Jiang, Shenzhen University, China

Conference Venue

Tiangang Xiyue Hotel Ningbo Jiangdong
天港禧悦酒店（宁波东部新城国际会展中心店）



地址：中国浙江省宁波市鄞州区（原江东区）惊驾路 1088 号

Address: No. 1088 Jingjia Road, near Century Avenue, Ningbo, China

住宿协议价：豪华双床房/豪华大床房　339 元含早

订房联系：崔洁琳经理 13857402241 （报 ICCSD 2026）

Guideline & Tips

Onsite Attendance

Oral Presentation

- Invited Talk Timing: a maximum of 20 minutes in total, including 3 minutes for Q&A. Please make sure your presentation is well timed.
- Oral Timing: a maximum of 15 minutes in total, including 3 minutes for Q&A. Please make sure your presentation is well timed.
- The conference is equipped with data projectors with a standard VGA connector. The speakers could also bring and use their own laptops or other presentation devices. Please check the compatibility of your laptop and the project before the session starts.
- Videos: If your Power Point files contain videos, please make sure that they are well formatted and connected to the main files.

Important Notes

- Please wear formal clothes or national characteristics of clothing.
- Please take care of your belongings during the conference. The conference organizer does not assume any responsibility for the loss of personal belongings of the participants.
- Please wear your participation badge during the conference. There will be NO access for people without a badge. NEVER discard your badge at will.
- Accommodation is not provided. Delegates are suggested to make early reservations.
- Please show the badge and meal coupons when dining. Please be advised that lost coupons will not be replaced.

Online Attendance

Platform

ZOOM, Download link:
https://zoom.us/download
https://zoom.com.cn/download (for Chinese authors)

Time Zone

Beijing Time: UTC/(GMT+8)

Online Meeting Room

Online Room: ID: 848 3029 5608 | Room Link: https://us02web.zoom.us/j/84830295608

Online Meeting Needs

- ✓ A computer with internet connection and camera
- ✓ Headphone/earphone
- ✓ A quiet place
- ✓ Stable internet connection
- ✓ Proper lighting and background

Test Your Presentation

Date: November 13, Friday, 11:00-12:00 (GMT+8)
Prior to the formal meeting, online presenters shall join the test room to ensure everything is on the right track.

Conference Recording

The whole conference will be recorded. We appreciate you proper behavior and appearance.

Tutorial

Time	09:00-12:00, Nov. 14, 2026
Venue	3 楼，君悦厅 (Jun Yue Hall, 3F)



Christos P. Sotiriou

University of Thessaly and Silicon Highway Technologies GP, Greece

Bio.: Christos P. Sotiriou received his BEng in Computer Science and Electronics, and PhD degree in Computer Science from the University of Edinburgh, Scotland, in 2001. He is currently a Professor at the Department of Electrical and Computer Engineering of the University of Thessaly and co-founder of Silicon Highway Technologies. His research include design methodologies for synchronous or asynchronous digital circuits and systems, Electronic Design Automation (EDA) Algorithms, Tools and Flows for digital circuit implementation, timing analysis, physical design, lower-power design, reliability and Power, Performance and Area (PPA) optimisation. Prof. Sotiriou has received three Qualcomm Faculty Awards, in 2019, 2020 and 2021. He has collaborated with several large corporations on EDA tools and flows development, circuit implementation and physical design. He is currently working on open-source EDA as part of the EU ODE4EC project (https://ode4ec.eu/), and is actively driving EDA R&D.

Title: The refEDA Tool Suite

Abstract: The refEDA tooset (https://github.com/Circuits-and-Systems-Lab-CASlab/refEDA) is an EDA suite including (1) an STA engine, (2) a Power analysis engine, (3) Physical design engines, including Global Placement, Detailed Placement and Legalisation, (4) a partitioning engine for divide and conquering, block based design and 3DICs, (5) an SET/SEU (Single Event Transient/Single-Event Upset) engine, capable of performing glitch analysis and glitch propagation for space electronics, (6) a RADHARD legaliser, capable of spacing out specific cells, e.g. majority voters, on a layout, to avoid them being affected by the same particle strike, an (7) Asynchronous circuit STA engine, and (8) Timing optimisation engines for improving TNS and WNS. (SDP?)

The goal of the ICCSD2026 tutorial is to showcase the capabilities of the refEDA tool suite in practical EDA flows, specifically: (1) pre/post-placement/post-parasitic extraction STA analysis, (2) STA vs SPICE for individual RC nodes or paths, (3) a pre/post-placement Power analysis flow, (4) a 3DIC flow for placement-partitioning achieving WL and improvements, (5) an SET flow achieving SET probability annotation and mitigation by trading off circuit area for reliability, (6), an SEU measurements flow, (7) a RADHARD Legalisation flow for satisfying spacing constraints and (8) a flow for Asynchronous circuit STA and optimisation.

Afternoon Session 1

Host	**Weikang Qian, Shanghai Jiao Tong University, China**		
Time	13:30-15:10, November 14, 2026	**Venue**	3 楼，君悦厅 （Jun Yue Hall, 3F）

Invited Speaker



Kang Zhao

13:30-14:00

Beijing University of Posts and Telecommunications, China

个人简介：赵康，教授，国家万人领军科技人才。2009 年博士毕业于清华大学 EDA 实验室，之后留校工作两年。2011 年加盟英特尔，参与 Intel 处理器、软硬协同等项目。2016 年加盟赛灵思公司，主导 Vitis 核心产品，对接 FPGA 领域的 EDA 工具。2022 年加盟北京邮电大学集成电路学院，专注 EDA 方向。以项目负责人身份牵头十四五科技部重点研发项目 1 项，国家自然基金项目 1 项。

报告题目：《FPGA 的敏捷设计与智能设计》

摘要：随着芯片设计迭代的速度越来越快，上市的窗口期越来越小，高层次综合技术被认为是达到敏捷设计开发的一条有效捷径。高层次综合主要面向软件工程师，自动将 C/C++高层次描述转换为合适的硬件 RTL 描述，并在 FPGA 上进行原型验证。此外，针对 AI 芯片异构架构的敏捷设计也是研究热点之一。报告将介绍高层次综合的关键难点，同时介绍我们团队在异构智能计算、智能体驱动 EDA 方面的已有基础。

Invited Speaker



Yuanqing Cheng

14:00-14:20

Beihang University, China

个人简介：成元庆，北京航空航天大学集成电路科学与工程学院长聘副教授，博士生导师。2013 年底加入北京航空航天大学，主要研究三维集成电路设计自动化和基于新型半导体技术的低功耗、可靠性设计。在该领域，申请人发表了包括设计自动化顶级会议和期刊 DAC，ICCAD，TCAD，PIEEE 等在内的论文 50 余篇，担任集成电路设计自动化专业会议 ICCAD/DATE/ASPDAC 的程序委员会委员，IFIP（国际信息处理联合会）10.5 工作组执行委员，IEEE CEDA 北京分会秘书，Elsevier 旗下 Integration, the VLSI Journal 期刊三维集成电路物理设计方向编委。主持

过包括国家自然科学基金、北京市自然科学基金，中科院先导专项等多项国家或省部级科研项目，并承担与华为海思半导体、燧原科技、立芯科技等公司在三维集成电路设计领域的多项校企合作项目。2017 年荣获北京市科技进步二等奖 1 项。2020 年在集成电路设计自动化权威会议 ASP-DAC 上组织“单片三维集成电路设计”论坛，荣获“卓越组织奖”。同年，在计算机学会首届 CCF 设计自动化年会上，作为论坛主席组织了“2.5D/3D 集成电路设计技术”论坛。2021 年指导学生参加 EDA 精英挑战赛，获得新思科技杯“2.5D 设计最优化布局”第一名和全国一等奖。2023 年荣获 EDA 顶会 ICCAD 的最佳论文提名奖。现为 IEEE 高级会员。

报告题目：基于 2.5D/3D 集成电路的仿真与验证

摘要：本报告围绕 2.5D/3D 集成电路的时序分析、热仿真与电源完整性三大关键问题，系统介绍了相关研究进展与技术成果。在时序分析方面，通过迁移学习、主动学习、矩阵补全及分层 GNN 等方法，实现了多工艺角时序的可信预测、稀疏重建和三维结构感知，有效降低了复杂工艺组合带来的分析开销；在热仿真方面，结合多保真学习、物理场代理、扩散模型和贝叶斯优化，实现了少样本条件下的快速热场预测、二维/三维温度重建及微通道液冷设计；在电源完整性方面，构建了涵盖 IR-drop 快速预测、高频 PDN 建模、多端口去耦优化和芯粒局部复用的完整方法体系。总体而言，相关工作形成了面向先进异构集成芯片的快速预测、物理建模、可信重建和协同优化能力，为降低设计验证成本、提升系统可靠性及支持芯粒化复用提供了重要技术基础。

Invited Speaker



Yujie Wang **14:20-14:40**

Institute of Computing Technology, Chinese Academy of Sciences, China

个人简介：中国科学院计算技术研究所副研究员。从事 2.5D/3D 芯片设计、先进封装以及 EDA 工具。作为任务负责人完成多款处理器芯片设计和流片工作，其工作成果作为主要交付物完成了重大科技项目交付验收。主持国家自然科学基金项目、之江实验室科研攻关项目子课题等。在 DAC、ICCAD、TVLSI 等集成电路会议、期刊上发表多篇论文。

报告题目：芯粒处理器架构-封装协同设计

摘要：芯粒设计中，封装已成为架构设计必须考虑的约束来源。封装涉及热效应、热机械应力等多物理场效应。如何打通物理场分析与架构优化是一项核心难题。本报告将介绍讲者在架构—封装协同设计方面的工作，主要包括：如何将封装中的电学仿真与热机械应力仿真融入架构仿真流程。

Oral Presentation

Paper ID: D2489 14:40-14:55

Title: A 48V to 2 ~ 5 V 95.1%-Peak-Efficiency Dual-Path Fibonacci-based Hybrid Converter with Inductor Current Reduction

Author(s): Ninghuang Li, Tao Xia, Jiayoon Ru

Presenter: **Ninghuang Li**, Peking University, China

Abstract: This paper presents a dual-path Fibonacci-based Hybrid (DPFH) converter targeting direct 48 V to 2 ~ 5 V with high peak efficiency and high power density. By fully leveraging flying capacitors through an optimized routing scheme, the proposed Fibonacci switched-capacitor (SC) topology successfully delivers an ultra-low voltage conversion ratio. In addition, the creation of a flying-capacitor-assisted current path relaxes the current stress on inductor, thereby yielding significant power efficiency gains. Implemented in a 180-nm BCD process, the converter delivers a maximum load current of 3A. Simulation results show that the converter achieves a peak efficiency of 95.1%.

Oral Presentation

Paper ID: D5767 14:55-15:10

Title: A Neural Encryption IP Core with Joint Adversarial Training Against Four Types of Attackers

Author(s): Zhenhao Guo, Yuejun Zhang, Huihong Zhang, Xinyu Li, Qikang Li, Qingxin Xie

Presenter: **Zhenhao Guo**, Ningbo University, China

Abstract: With the emergence of neural cryptography, adversarial neural networks have provided a new paradigm for end-to-end encryption and decryption. This paper presents a multi-attacker adversarial neural network encryption IP core. The proposed design is initialized with pretrained parameters of Alice and Bob, followed by fixed-point quantization and joint adversarial optimization against multiple attackers. Experimental results demonstrate that Bob achieves a bit-wise decryption accuracy of 99.99%, while the decryption accuracies of all attackers remain around 50%, corresponding to the random-guessing level. Moreover, the generated ciphertext successfully passes randomness tests, indicating favorable statistical properties. The proposed IP core is further synthesized, placed, and routed using a TSMC 28-nm CMOS process. Hardware–software co-design results show that the proposed architecture achieves a favorable tradeoff among communication reliability, security evaluation capability, and resource-efficient hardware implementation.

Afternoon Session 2

Host	Yuanqing Cheng, Beihang University, China		
Time	15:40-17:30, November 14, 2026	Venue	3 楼，君悦厅 (Jun Yue Hall, 3F)

Invited Speaker



Xiaole Cui

15:40-16:00

Peking University ShenZhen Graduate School, China

个人简介：崔小乐，北京大学深圳研究生院教授，从事 IC 设计、电路可测性/可靠性/安全性研究。已发表学术论文 200 余篇，拥有授权发明十余项。担任 CCF 容错计算专委、集成电路设计专委执行委员、中国指挥控制学会可靠性技术专委会委员、中国测试计量学会集成电路测试专委委员等。现任 IEEE P3405、P3468 等标准的工作组成员。

报告题目： Chiplet 互连测试与修复技术进展

摘要：介绍 IEEE P3405 标准的开发进展，并介绍北京大学深圳研究生院在 Chiplet 互连测试与修复技术方面的工作进展，涉及 TSV Pre/Post-bond 测试、测试调度、TSV 故障修复、串扰抑制编码、SerDes 故障诊断、3D Mesh NoC 功能测试等。

Invited Speaker



Weikang Qian

16:00-16:20

Shanghai Jiao Tong University, China

个人简介：钱炜慷，上海交通大学浦江国际学院长聘副教授，博士生导师。主要研究领域为面向新型计算范式的电子设计自动化和数字电路设计。其研究成果曾获 EDA 领域顶级会议 ICCAD 最佳论文提名三次以及 DATE 最佳论文提名两次。现任 IEEE TCAD 副编辑。现为 IEEE 高级会员、CCF 高级会员、CCF 集成电路设计专委会执行委员。

报告题目：机器学习辅助的逻辑综合

摘要：随着集成电路设计复杂度的持续攀升，传统逻辑方法在效率与优化质量上面临严峻挑战。机器学习技术为逻辑综合提供了全新的解决方案。本报告将介绍本课题组开展的两个工作：GUALO 和 YOCO。其中，GUALO 面向工艺无关综合任务，提出了一种基于对比学习和不确定性感知的逻辑综合序列寻优方法，进一步提升了综合质量。YOCO 面向工艺映射任务，提出了一种基于目标检测算法 DETR 的框架，直接预测电路中高质量的候选切割以替代传统枚举流程，减少了冗余计算。

Invited Speaker



Xiaohang Wang

16:20-16:40

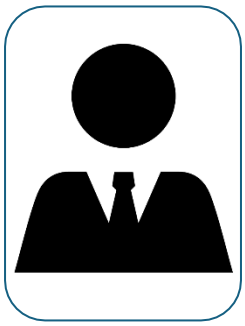
Zhejiang University, China

个人简介：王小航，浙江大学计算机学院/网络空间安全学院教授，入选国家级青年人才。发表包括 IEEE/ACM Trans 顶级期刊和 Micro、DAC 顶级会议在内的论文 80 余篇，获得包括 VLSI-SoC 在内的两项芯片设计与硬件安全领域著名会议最佳论文奖。主持科研项目 20 余项，国家级 7 项，担任片上网络领域知名会议 NoCS 18/22 分会组织者，CCF DAC 2023 组织委员会副主席，CCF 芯片大会论坛主席，NoCArc 18 指导委员会委员，APCCAS 18 分会主席，ICCAD、CF（CCF B 类会议）TPC 成员，在 ICCS 20 做特邀报告并担任程序委员会主席，在 20、21 年 CCF 容错计算年会分论坛做特邀报告，担任 Mathematics（JCR 一区）、Computers and Electrical Engineering、Integration, the VLSI Journal 等期刊客座主编，计算机技术与发展期刊的专题编委，担任中国计算机学会（CCF）容错计算、集成电路专委的委员。

报告题目：集成芯片仿真方法与设计空间探索

摘要：大模型时代对算力需求急剧增加，集成芯片成为重要的算力底座。然而，集成芯片设计空间相较传统单芯片急剧增加，需要仿真器以支撑前期设计空间探索。然而，现有的仿真器无法模拟异构芯粒的快速、灵活集成，因此本报告首先对我们研发的 LEGOSIM：异构芯粒集成芯片仿真器进行介绍，其次介绍片内片间互连子系统、存储子系统优化，以探索集成芯片的设计空间。

Invited Speaker



Xueyin Zhang

16:40-17:00

Shanghai Hongxin Micro Nano Technology Co., Ltd., China

报告题目： 鸿芯微纳 Komponist® 3DIC 设计平台

摘要：本次演讲系统介绍了鸿芯微纳（GIGA Design Automation）自主研发的 Komponist® 3DIC 设计平台，该平台覆盖从系统规划、物理实现到签核的完整 3DIC 设计流程。平台协同 Partita® 层次化设计、Fantaisie®布局布线、ChimeTime®静态时序分析、HesVesPower®功耗分析及热分析引擎，通过统一数据库实现系统级与芯片级布局的双向实时同步。

在系统规划层面，Komponist 支持自动 Feedthrough 插入、TSV 规划、IO 优化、芯片堆叠及 2.5D 中介层设计（含 HBM 自动布线与 UCIe 高速 D2D 自动布线），并原生支持 3Dblox 2.0 标准与背面设计（Backside Design）。平台内置材料管理器和模型生成器，可与第三方分析引擎

无缝集成，同时提供 3D 时序调试器以加速关键路径收敛。通过案例分享，展示了 3D 设计在保持标准单元数量几乎不变的前提下，芯片面积可缩减 24%–43%，时序性能（TNS）显著优于传统 2D 方案。平台将持续推进 3D 布局布线协同优化、混合键合优化 I 及 3D 异构集成等前沿能力，助力国产先进封装 EDA 生态建设。

Oral Presentation

Paper ID: D9170 17:00-17:15

Title: A 75 F^2 Leakage-Current Based Physically Unclonable Function With Unstable-Bit Screening Function

Author(s): Zhenghe Wang, Hui Li, Gang Li, Xuejiao Ma, Tianyi Xiao

Presenter: **Zhenghe Wang**, Wenzhou University, China

Abstract: A physically unclonable function (PUF) is a novel hardware security primitive that extracts random process variations arising during chip fabrication to generate physically unclonable hardware fingerprints, and thus has significant application value in the field of information security. To address the large area overhead and insufficient response stability of weak PUFs, this paper proposes a leakage-current based PUF with unstable-bit screening function. Applying a bias voltage to the sources of minimum-sized NMOS transistors keeps them operating in the subthreshold region. This converts small threshold-voltage mismatches into more distinguishable differences in subthreshold leakage current, which a sense amplifier compares to generate PUF output responses. In addition, applying different bias voltages to the sources of different entropy-source transistors within a PUF cell allows its response stability to be assessed and unstable bits to be flagged. The proposed PUF is implemented in a TSMC 65 nm process, with a PUF cell feature size of only 75 F2. Chip measurements show good randomness (50.12%), uniqueness (50.214%), and reliability (0.273%). A zero bit error rate is achieved in the output responses with a false-marking rate of no more than 8%.

Oral Presentation

Paper ID: D7164 17:15-17:30

Title: A Four-Coefficient-Parallel BRAM-Free NTT Architecture With Dual-Bank Commutation and Interstage Overlap for ML-DSA

Author(s): Baomin Tang, Yuejun Zhang, Qingxin Xie, Qikang Li

Presenter: **Baomin Tang**, Ningbo University, China

Abstract: This work proposes a four-coefficient-parallel BRAM-free NTT/PWM/INTT architecture for ML-DSA. A dual-bank commutator based on two local 1R1W banks reorders and re-pairs the input stream to continuously feed two parallel BFUs without multi-port memory conflicts. A dependency-aware interstage-overlap strategy further reduces transform latency by allowing each stage to start once its required operands are available. NTT and INTT share the same bidirectional pipeline, while BFU and final-stage multiplier reuse improves resource utilization. Implemented on a Xilinx Artix-7 FPGA, the design completes a 256-point NTT/INTT in 163 cycles, corresponding to 1.417 μs at 115 MHz, with zero BRAM usage. Compared with an existing zero-BRAM design, DSP usage is reduced by 67.2%, while LATP and FATP are reduced by 31.4% and 62.0%, respectively.

Online Session (GMT+8)

ROOM	Room: ID: 848 3029 5608 | Room Link: https://us02web.zoom.us/j/84830295608
Time	16:00-17:00, November 15, 2026

Oral Presentation

Paper ID: D1846 **16:00-16:15**

Title: A Compact Incremental Delta-Sigma ADC for Column-Parallel Terahertz Readout

Author(s): Jingwu Gong, Jiekun Zhang, Suzhen Cheng, Zhongxu Sun, Nan Liu, Peng Ding, Zhanqiang Ru, Jiandong Sun, Hua Qin, Helun Song

Presenter: **Jingwu Gong**, Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences

Abstract: A compact incremental delta-sigma analog-to-digital converter (DS ADC) is presented for a 320×240 terahertz readout array with an 80 μm column pitch. The ADC combines a third-order feed-forward modulator with programmable oversampling and an on-chip timing controller that aligns reset release with the sampling phase and controls the conversion window length. An on-chip current source provides the bias for normal operation, while a selectable external source allows bias current sweeps during characterization. Fabricated in 0.18 μm CMOS, the ADC core occupies 0.0456 mm2 with a width of 71 μm. At a 2-MHz ADC clock, oversampling ratios (OSRs) of 128 and 256 yield an effective number of bits (ENOB) of 11.6 and 13.8, respectively. At OSR = 256, the differential and integral nonlinearities are -0.47/ + 0.54 and −1.44/ + 1.17 LSB, respectively, for a 14-bit output code mapping. The modulator consumes 265 μW from a 3.3-V supply at a 10 μA bias setting. External bias sweeps show diminishing ENOB improvement at higher currents, while the maximum differential and integral nonlinearities vary less with further increases in bias current above approximately 8 μA.

Oral Presentation

Paper ID: D8113 **16:15-16:30**

Title: Design of a High-Speed and Low-Power Readout Circuit for UTBB-Based Image Sensors

Author(s): Xiaoyu Zhong, Liang Yang, Jian Shao, Yang Gao

Presenter: **Xiaoyu Zhong**, The 58th Research Institute of CETC, China

Abstract: This paper presents a high-speed, low-power column readout circuit for ultra-thin-body and buried-oxide (UTBB)-based single-transistor image sensors with threshold-voltage-modulated sensing. Clamp circuits and a global ramp generator encode threshold-voltage shifts induced by photogenerated charge into time-domain information, which is subsequently digitized by a single-slope analog-to-digital converter (SS-ADC). To further reduce power consumption and improve readout performance, an op-amp-free bandgap reference and a two-stage static comparator are also developed. A test chip was fabricated in a 55 nm CMOS process and experimentally characterized. At a 10-bit nominal resolution, the row readout time is 3.7 μs, and the local per-column readout power is 64.2 μW. The measured output noise is 2.1-2.2 LSBrms, corresponding to a noise-limited effective resolution of approximately 8.9 bits. The measured differential nonlinearity (DNL) ranges from -0.72 to +1.12 LSB, while the integral nonlinearity (INL) ranges from -0.28 to +0.66 LSB. The proposed circuit enables fast row readout while balancing speed, power consumption, and column-to-column consistency.

Oral Presentation

Paper ID: D4653 **16:30-16:45**

Title: A High-Voltage High-Slew-Rate Rail-to-Rail Operational Amplifier with Constant Transconductance

Author(s): Bin Wang, Hanjie Hou, Yang Zong

Presenter: **Bin Wang**, Shenyang University of Technology, China

Abstract: This paper presents a 36 V rail to rail operational amplifier for high voltage analog signal processing in harsh environments. A complementary MOS and BJT composite differential input stage extends the common-mode input range and increases the input transconductance. A current-compensation network maintains approximately constant transconductance as the input common-mode voltage moves from the negative to the positive supply rail. The intermediate stage uses a folded-cascode topology, while the output stage adopts a common-source Class AB structure to combine high gain, large output swing, and low quiescent power. Miller and cascode compensation are jointly applied for frequency stabilization, and a selectively triggered slew-rate enhancement circuit supplies additional charging or discharging current during large-signal transitions. The circuit is designed in a 0.18 micrometer Huahong high voltage process and evaluated with Cadence Spectre simulations. Under a 36 V supply, 50 pF load capacitance, and 2 kilohm load resistance, the amplifier achieves a 128.5 dB dc gain, 69.7 degree phase margin, 8.36 MHz unity-gain bandwidth, and 1.5 mW quiescent power at 27 degrees C. The simulated common-mode input range is 0 to 36 V and the output swing is 45.59 mV to 35.76 V. Across minus 40 to 125 degrees C, the dc gain remains above 120 dB. With slew-rate enhancement, the simulated slew rate increases from 0.3 to 10 V per microsecond.

Oral Presentation

Paper ID: D4560 **16:45-17:00**

Title: PCB Design and Verification of an MP4560-Based DC-DC Step-Down Module

Author(s): Haojie Huang, Yongbo Liao

Presenter: **Haojie Huang**, University of Bristol, United Kingdom

Abstract: This project used MPS DC/DC Designer Online to simulate and designa DC-DC buck converter module based on the MP4560DN-LF-Z. The chip has a specified input voltagerange from 3.8 V to 55 V, integrates a 250 mΩ power MOSFET, and supports switching frequencies up to 2 MHz. TThe module was designed for a 3.3 V output and a maximum output current of 2 A. First, a simulation was carriedd out using the MPS Online tool, then complete the schematic design, component selection and PCB layout and routing planning. In terms of circuit design, the module used a 4.7 uF and a 100nF capacitor to form an input decoupling network, in order to reduce input voltage fluctuations. A 10 µH power inductor wiith a rated current of 3.2 A and a Schottky diode formed the buck power circuit. A 22 LE and a 100 nF capacitors were set at the output for output filtering and to supply power during load transients. When the feedback voltage of the IMP4560 is approximately 0.8 V, the theoretical output voltage is calculated as follows: This result is close to the design target of 3.3 V indicated in theschematic. The module was equipped with a USB Type-C 6-pin connector and a 2.54 mm pin header as input cornnection options, along with screw terminals and pin headers as output interfaces to cater for both experimental debugging and practical wiring requirements. PCB design focused on high-frequency switching current paths, the positioning of input bypass capacitors, the width of power copper traces, immunity of feedback signals to interference, and heat dissipation capabilities. The input capacitors should be placed as close as possible to the VIN and GNDpins of the MP4560. The switching-node copper area should be limited, and feedback traces should be routed away from the SW node and the inductor. Large ground copper pours and the chip's exposed thermal pad help reducbe conduction losses and device temperature In the no-load test, the measured input and output voltages were5.160 V and 3.248 V. The output was approximately 1.58% below the 3.3 V design target, verifying the basic step-dowvn function of the prototype.